ABSTRACT

A method and apparatus for monitoring the performance characteristics of a multithreaded processor executing instructions from two or more threads simultaneously. Event detectors detect the occurrence of specific processor events during the execution of instructions from threads of a multithreaded processor. Specialized event select control registers are programmed to control the selection, masking and qualifying of events to be monitored. Events are qualified according to their thread ID and thread current privilege level (CPL). Each event that is qualified is counted by one of several programmable event counters that keep track of all processor events being monitored. The contents of the event counters can then be accessed and sampled via a program instruction.